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Fabrication of air-stable n-type carbon nanotube thin-film transistors on flexible substrates using bilayer dielectrics†

Guanhong Li,[a,b] Qunqing Li,*[a,b] Yuanhao Jin,[a,b] Yudan Zhao,[a,b] Xiaoyang Xiao,[a,b] Kaili Jiang,[a,b] Jiaping Wang[a,b] and Shoushan Fan[a,b]

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Single-walled carbon nanotube (SWNT) thin-film transistors hold great potential for flexible electronics. However, fabrication of air-stable n-type devices by methods compatible with standard photolithography on flexible substrates is challenging. Here, we demonstrated that by using a bilayer dielectric structure of MgO and atomic layer deposited (ALD) Al_2O_3 or HfO_2, air-stable n-type devices can be obtained. The mechanism for conduction type conversion was elucidated and attributed to the hole depletion in SWNT, the decrease of the trap state density by MgO assimilating adsorbed water molecules in the vicinity of SWNT, and the energy band bending because of the positive fixed charges in the ALD layer. The key advantage of the method is the relatively low temperature (120 or 90 °C) required here for the ALD process because we need not employ this step to totally remove the absorbates on the SWNTs. This advantage facilitates the integration of both p-type and n-type transistors through a simple lift off process and compact CMOS inverters were demonstrated. We also demonstrated that the doping of SWNTs in the channel plays a more important role than the Schottky barriers at the metal contacts in carbon nanotube thin-film transistors, unlike the situation in individual SWNT-based transistors.

Introduction

Single-walled carbon nanotubes (SWNTs) are promising materials for future electronic applications because of their extraordinary properties, including high mobility,[1] and large current density.[2] High performance integrated circuits[3–6] and a demo computer[7] have been demonstrated based on individual SWNTs and SWNT random networks. The transistor dimension has been scaled down to 10 nm, and ballistic transport has been represented.[8] Compared with individual nanotubes, a thin film of SWNT random networks shows better device-to-device uniformity by statistical averaging of a large number of SWNTs. Moreover, SWNT random networks are suitable for fabricating thin-film transistors (TFTs) on flexible substrates because of the high fracture strains, up to 30%.[9] Carbon nanotube thin-film transistors (CNT-TFTs) well surpass polycrystalline-silicon-based TFTs with low-cost, and surpass amorphous silicon and organic semiconducting transistors in terms of mobility.[10]

To achieve low static power consumption and high noise margin, both p-type and n-type transistors are needed to make complementary logic circuits. However, whether for TFTs or individual-SWNT-based transistors, fabricating air-stable n-type devices is challenging because the as-made devices are p-type under ambient conditions. Many strategies have been investigated to realize n-type conduction. One approach is doping the SWNT channel or the metal–SWNT contacts with alkali metal atoms such as potassium,[11,12] or organic polymers such as polyethylene imine[13] and viologen.[14] Nevertheless, the organic molecules are unstable and cannot be patterned by the lithography process, and the metal atoms are vulnerable to oxidation. Another approach is using rare earth metals such as Gd, Sc, Y, or Er.[15–18] These metals have low work-function and good binding affinity with SWNTs; they could thus make Ohmic contact with the conduction band of SWNTs, allowing direct electron injection. However, this method is not applicable to CNT-TFTs directly. Recently, several groups have reported air-stable n-type transistors by vacuum annealing followed by passivation with Si_3N_4 film[19,20] or atomic layer deposited (ALD) high-κ dielectrics.[21,22] The pre-growth heating process desorbs oxygen adsorbates and the passivation layer isolates the clean channel from ambient air. Moreover, the

[a]*State Key Laboratory of Low-Dimensional Quantum Physics, Department of Physics & Tsinghua-Foxconn Nanotechnology Research Center, Tsinghua University, Beijing 100084, China. E-mail: qunqli@mail.tsinghua.edu.cn*
[b]*Collaborative Innovation Center of Quantum Matter, Beijing, China*
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high-κ layer also introduces positive fixed charges in the vicinity, thus electrostatically dopes the SWNT channels. However, this method suffers from relatively high temperature, which is not compatible with the standard lift-off process in semiconducting techniques and cannot be applied to flexible plastic substrates. In addition, partially oxidized yttrium[23] was also reported to have doping effects on SWNT in the further oxidation process. However, the consistency is unsatisfactory and the result is sensitive to evaporation and oxidation conditions because of the highly reactive nature of the material.

Therefore, a method for fabricating n-type SWNT TFT is urgently needed. This method should not require high temperature process, be compatible with standard silicon techniques and applicable to flexible substrates, and be consistent, reproducible, and stable.

In this work, we show that air stable n-type CNT-TFTs can be fabricated at low temperature of 120 °C or 90 °C by utilizing bilayer dielectrics of MgO and an ALD high-κ dielectric. Using this method, we have successfully fabricated n-type CNT-TFTs on flexible polyethylene terephthalate (PET) substrates. The as-fabricated n-type CNT-TFTs have on/off ratios of 4×10^3 and 3×10^5 on flexible substrates and on silicon substrates, respectively, and the corresponding ratios between n-branch on-current and p-branch on-current (I_{on_n}/I_{on_p}) are 5×10^2 and 7×10^4 respectively. The n-type device fabricated by this method shows good stability in air, and the electronic properties do not vary over time for up to 104 days. The change in carrier type is attributed to the reduction of charge trap states near the conduction band of SWNT by MgO together with energy band bending due to positive fixed charges in the ALD dielectric.

Results and discussion

A schematic architecture of our fabricated flexible n-type TFT utilizing bilayer dielectrics of MgO and ALD high-κ dielectrics is illustrated in Fig. 1a. A PET sheet serves as the flexible substrate. On top of the PET substrate, a silicon oxide layer of 50 nm is deposited by e-beam evaporation. The surface of the SiO_2 layer is functionalized with aminopropyltriethoxysilane (APTES) to act as an adhesion layer for SWNTs. The uniform SWNT film is obtained by immersing the functionalized substrate into SWNT solutions. We used pre-separated SWNTs with a semiconducting SWNT purity of 99%. A typical SEM image of the SWNT film on the PET substrate is shown in Fig. 1b. Drain–source electrodes of gold were defined by photolithography and lift-off after SWNT film formation. Ten nanometers of MgO and 30 nm of Al_2O_3 were then deposited using e-beam evaporation and ALD, respectively, to serve as the bilayer gate dielectric. This bilayer structure is a peculiar feature of our method. The use of bilayer dielectric enables us to achieve conduction type change at a relatively low temperature of 120 °C, which is equal to the temperature for baking of a photoresist in the photolithography process. Therefore, the method is compatible with the standard lift-off process in silicon semiconductor techniques. This compatibility allows us to pattern the device in a 2-dimensional plane

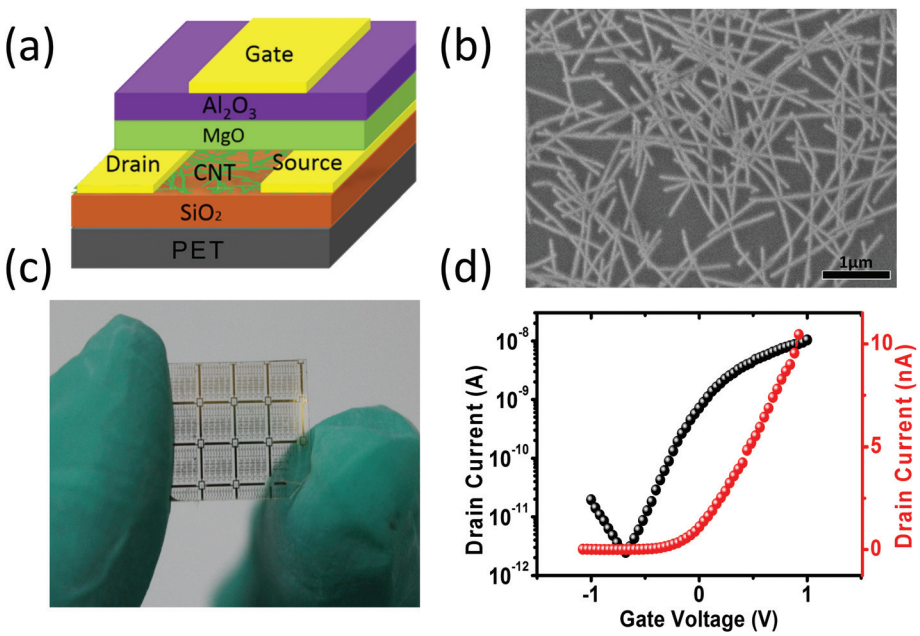

Fig. 1 n-Channel top-gated CNT-TFTs with MgO/Al_2O_3 dielectrics on a flexible PET substrate. (a) Schematic diagram of the flexible n-type CNT-TFTs. (b) SEM image of the SWNT thin film. (c) Optical image of n-type TFT arrays on a thin sheet of PET. (d) Transfer characteristics of a typical flexible CNT-TFT measured at V_{DS} = 1 V with top-gate voltage swept from –1 to 1 V, showing n-type electrical transport. Both the channel length and width are 40 μm. The thickness of MgO and Al_2O_3 are 10 nm and 30 nm respectively.

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using the lift-off process, avoiding etching the gate dielectric. This is a significant improvement compared to earlier reported approaches for a carrier type change using individual ALD high-κ dielectrics, which require a relatively high temperature of 250 °C; thus, an additional etching process to expose the electrodes beneath the ALD dielectric is needed. In particular, the etching operation will make the overall process flow complicated when fabricating CMOS integrated circuits with top-gate configuration because the etching of the ALD dielectric will damage most kinds of materials (especially, any oxides) below the dielectric. Most importantly, 120 °C is a temperature that flexible substrates, such as PET, can tolerate. This enables complementary circuits on flexible substrates. The channel area of the TFT is 40 μm × 40 μm, which is defined by photolithography and oxygen plasma etching before the formation of the dielectric. The mean diameter of the SWNTs is 1.4 nm. The top gate electrode metal is Ti/Au. Fig. 1d shows the drain current (I_{DS}) as a function of gate–source voltage (V_{GS}) for a typical top-gated flexible n-type CNT-TFT on both linear (red) and logarithmic (black) scales. A flexibility test (Fig. S6†) shows that our device still works after bending with a radius of 9 mm. The measurements were carried out under ambient conditions. Here, the drain–source (V_{DS}) bias was set at 1 V. As V_{GS} increased from negative to positive 1 V, the I_D increased by 3 orders of magnitude from about 2 pA to 10 nA. The ratio between the n-branch on-current and p-branch on-current is 5×10^2. This clearly shows that hole conduction is well suppressed in this device and confirms the success of our proposed approach for fabricating top-gated n-type TFTs on flexible plastic substrates. Furthermore, the threshold voltage (V_{th}) is approximately 0.08 V, which is very close to zero. The subthreshold swing (SS) is 248 mV per decade. It is worth noting that n-type conduction has also been reported before by Si_3N_4 passivation on flexible substrates.[24] However, a hard mask was used to pattern the Si_3N_4 area because of the relatively high temperature (200 °C) involved, which limited the patterning resolution of the method on the scale of 100 μm. Compared with this previous achievement, our method is compatible with the standard lift-off process facilitated by the relatively low temperature of 120 °C.

To investigate the mechanism for the carrier type change, we have conducted systematic experiments to study the impacts of the gate dielectric or channel passivation layers on the transport properties of CNT-TFTs. A series of TFTs with various dielectric layers were fabricated on hard silicon substrates for comparison. Before this, it's helpful to show the primary performance of the fabricated n-type transistors on a silicon substrate, for a basic understanding of the transistor properties. The fabrication process is the same as that on the flexible PET substrate, except for the substrate, where silicon with a thermal silicon oxide layer of 300 nm thick is used, as shown in Fig. 2a. The silicon substrate itself could act as a back gate electrode for the TFT because of its heavily doped nature. Therefore, the device can be measured by either the back gate or the top gate. Fig. 2b shows the transfer characteristics of the CNT-TFT measured with both the back gate (black) and the top gate (red). Both of them showed the same on/off ratios of 3×10^5 and the same I_{on_n}/I_{on_p} of 7×10^4. The

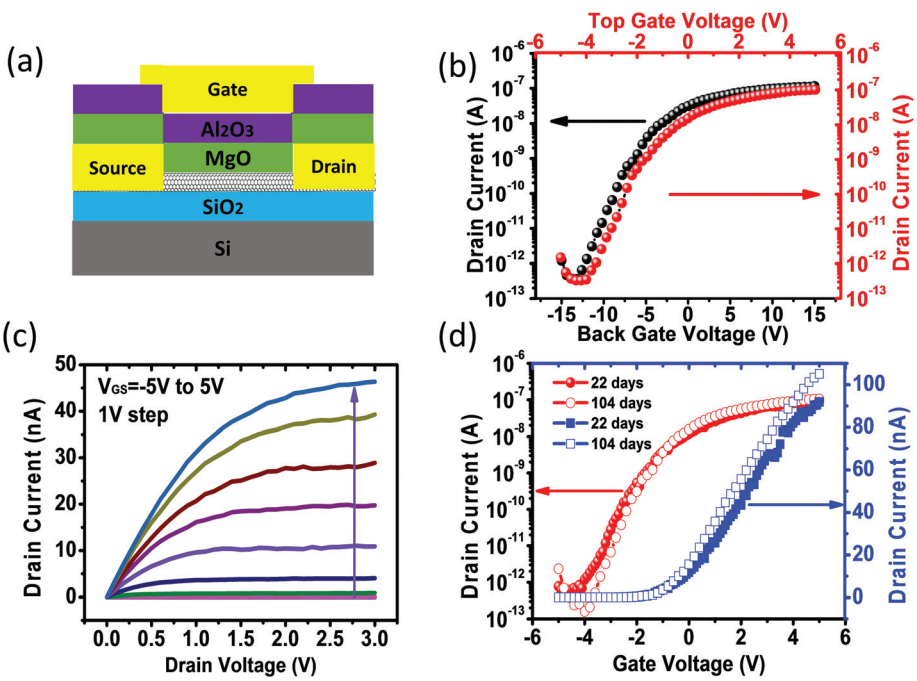

Fig. 2 Properties of the n-type TFT on silicon substrate. (a) Cross-sectional schematic of the device on silicon substrate. The thickness of MgO and Al_2O_3 are 10 nm and 30 nm respectively. The channel area is 40 μm × 40 μm. (b) Transfer characteristics of the TFT measured at V_{DS} = 2 V with the top gate (red) and back gate (black). (c) Output characteristics and (d) air stability of the device.

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on and off current also show no difference between the two measurements. This result means that the n-type conduction behaviour is an intrinsic property of the SWNT channel, regardless of whether the top or back gate is used. The difference in gate modulation efficiency originates from the relatively low capacitance of the back gate, because the subthreshold swing is determined by the dielectric capacitance and the trap state resulting capacitance as[25]

$$SS = \left(k_B T \frac{\ln(10)}{e}\right)\left(1 + \left(\frac{C_{it}}{C_g}\right)\right) \quad (1)$$

where C_g is the dielectric capacitance and C_{it} is the capacitance resulting from the trap state. Here, the SS is 593 mV per decade for the top gate transfer characteristics. The independence of conduction type on the gate used allows us to discuss the electrical characteristics of our devices using either the top gate or back gate.

The output characteristics are also shown in Fig. 2c. The drain voltage was applied from zero to 3 V, with the top gate voltage stepped from −5 V to 5 V. The linear transport property at low V_{DS} indicates a small contact barrier. The I_{DS} increases with increasing V_{GS} toward positive voltage. This clearly demonstrates that the TFT is n-type conduction. The long-term stability in air is an important performance index for n-type SWNT transistors because carbon nanotubes are prone to be hole-doped by the adsorbates in air. Here, our fabricated n-type CNT-TFT shows good stability. The electrical characteristics of the TFT remain nearly unchanged after storage under ambient conditions for 104 days, as shown in Fig. 2d. As the consistency and reliability of the process are also important, we provided the histograms of on-current, on/off ratio, V_{th} and the results of multiple devices from other batch (Fig. S1 and S2†). The performance change after n-doping is also presented for devices based on CNTs with different semiconducting purities (Fig. S3†). The average mobility is also evaluated for the devices using CNT with semiconducting purity as 98%, which is about 14.9 $cm^2\ V^{-1}\ s^{-1}$ (Table S1†), comparable to a recent report.[20]

To elucidate the validity of our proposed n-type transistor structure, we compared the electrical transport characteristics of devices with our proposed bilayer MgO/Al_2O_3 dielectric structure and devices with only an ALD Al_2O_3 single layer as the top gate dielectric. The two kinds of devices were located on the same wafer and went through the same fabrication process, except that a part was masked out to avoid deposition of MgO. The corresponding experimental results are shown in Fig. 3a. It can be seen that the device with a single layer of

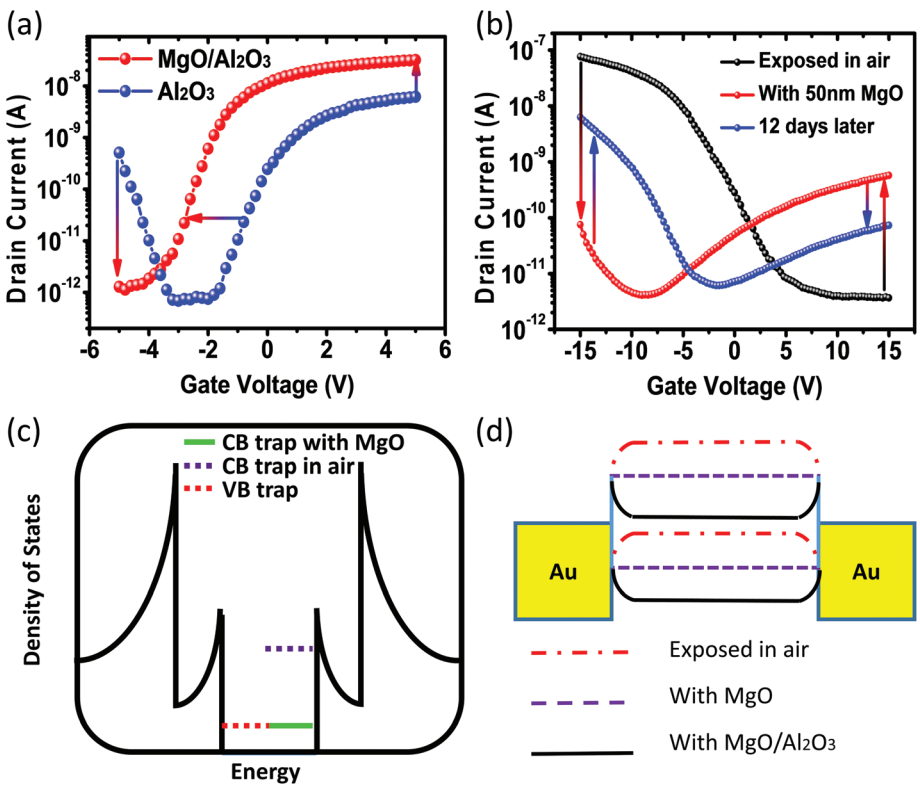

Fig. 3 Mechanism of n-type CNT-TFT with MgO/Al_2O_3 bilayer as top-gate dielectrics. (a) Transfer characteristics of CNT-TFT with single-layer ALD Al_2O_3 (blue) and MgO/Al_2O_3 (red) bilayer as top gate dielectrics. (b) Transfer characteristics of CNT-TFT with the channel exposed to air (black), just after deposition of 50 nm MgO (red) and 12 days after MgO deposition (blue). (c) Schematic illustration of the density of trap states near the band edge of CB and VB affected by MgO deposition. (d) Schematic of energy band diagram for the device exposed (red), with only MgO deposition (violet), and with MgO/Al_2O_3 (black) bilayer as dielectrics.

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120 °C deposited Al_2O_3 as dielectric shows ambipolar electrical transport characteristics, with electrons conducting at positive gate voltage and holes conducting at negative gate voltage. The hole conduction is slightly smaller than electron conduction. This ambipolar behavior is consistent with many published studies with an Al_2O_3 single layer as the gate dielectric or passivation layer. In contrast, the CNT-TFT with an additional thin layer of 10 nm e-beam evaporated MgO shows clear n-type conduction behavior. Compared with the Al_2O_3 device, the MgO/Al_2O_3 device shows 500 times lower hole conductance and 5 times higher electron conductance. The hole conduction is significantly suppressed with the addition of the MgO layer before ALD Al_2O_3.

With respect to the commonly observed p-type transport behavior of SWNT FETs exposed to air, the usual viewpoint is that the oxygen adsorbed on the SWNT channel and the Schottky barrier of SWNT–metal contacts retard the injection of electrons.[26,27] Experimental proof for this viewpoint is that n-branch conduction can be observed after annealing the exposed SWNT transistor in a vacuum at high temperatures for a long time. The increase in electron conduction is believed to result from oxygen desorption during the vacuum annealing process. However, water molecules also exist under ambient conditions and can also be desorbed by the vacuum annealing treatment. Thereby, the impact of water molecules also needs to be considered further.

A recent study has taken this previously ignored water molecule into account.[28] The study ascribes the suppression of electron conduction to charge transfer from the SWNT channel to an oxygen/water redox couple based on two experimental phenomena. First, SWNT transistors fabricated on hydrophobic parylene substrates can conduct electrons equally when exposed to air, unlike devices on the hydrophilic SiO_2 substrate. Second, for an ambipolar transistor on a SiO_2 substrate after annealing treatment in a vacuum, the reduction in electron conductance is very slight when exposed to either O_2 or H_2O alone. On the contrary, a significant decrease in electron current is observed when exposed to O_2 and H_2O simultaneously.

Our previous studies have also assumed that the numerous trap states near the SWNT conduction band edge have caused the poor gate modulation of electron conduction.[29] According to these reports, we assume that the co-existence of oxygen and water plays a dominant role in the suppression of electron conduction in CNT-TFTs. Also, carbon materials have been functionalized with metal oxide layers to tune the electrical properties.[30,31] Therefore, we propose the present bilayer dielectric structure to further remove the adsorbed water molecules in addition to desorbing oxygen by the ALD procedure. The MgO layer is thought to have three important functions in achieving n-type SWNT transistors in our present work.

First, magnesium oxide can act as a hygroscopic material, which could assimilate water and form magnesium hydroxide. This reaction represents alkalescency. We assume that the adsorbed water will be saturated after sufficient reaction with MgO because the quantity of MgO is excessive compared to the adsorbed water molecules. This saturated water has a pH value of 10.3. The Fermi level of the oxygen/water redox couple depends on the pH value of the oxygen solvated solution as[29]

$$E_{F,red} = -5.71 - 0.0148[\log(C_{ox}) - 4pH] \quad (2)$$

where C_{ox} is the solvated oxygen concentration, assumed to be saturated and thus constant. By differentiating this equation, we have

$$\Delta E_{F,red} = 0.0592\Delta pH \quad (3)$$

Therefore, the Fermi level of the oxygen/water layer will be raised by 195 meV, which is nearly one third of the SWNT band gap (0.6 eV for a diameter of 1.4 nm). So, the Fermi level of the SWNT will also be increased dramatically because the Fermi level should be equal between the SWNT and the redox couple when the system reaches equilibrium. Second, H_2O was used as the oxygen source for the deposition of Al_2O_3 by the ALD method. The pre-deposited MgO will prevent these water molecules from affecting the SWNT channel and the metal–SWNT contact. Third, assimilation of water molecules by MgO will reduce the ultimate amount of water in the vicinity of the SWNT channel. Because the charge transfer between the oxygen/water couple and SWNT is proportional to the effective water volume as $Q = qN_AV \times [c(OH^-) - c(H^+)]$,[29] a reduction in the amount of water molecules will alleviate the suppression function of the redox couple on electron conduction. Here, q is the elementary charge, N_A is the Avogadro constant, and V is the effective water volume. Furthermore, MgO is investigated in other reports as a candidate with high-κ dielectric with κ value of 9.8 and a wide band gap of 7.3 eV.[32] The choice of MgO as part of the bilayer dielectric causes no reduction in the gate modulation efficiency.

Although the introduction of MgO is thought to promote electron conduction in principle as described above, a single layer of MgO is unable to prevent water and oxygen molecules in air from penetrating the dielectric layer because of the relatively incompact material structure. The incompact nature originates from the deposition method, *i.e.*, e-beam evaporation. We have investigated the electrical property change of a device passivated with only 50 nm-thick MgO. The results are shown in Fig. 3b. The three curves represent the electrical characteristics of the same device at three different stages. When the back-gated transistor is exposed to air without MgO, it behaves in a perfectly p-type way. The electron conduction is completely suppressed by the oxygen/water couple. Conversely, after the deposition of the MgO layer, the n-branch current increases significantly by 2 orders of magnitude and the p-branch current decreased by 3 orders of magnitude. The device is changed to an ambipolar transistor by the deposition of the MgO layer. The SS for electron conduction and hole conduction are 6.8 V per decade and 4.2 V per decade, respectively. This result indicates that the introduction of the MgO layer has eliminated the suppression of electron conduction by the oxygen/water redox couple. However, this ambipolar behavior

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is not stable and degrades remarkably after 12 days as a result of water and oxygen molecule adsorption from ambient air.

According to a previous publication,[29] the influence of the oxygen/water couple can be equivalent to that of the large trap states. The parasitic capacitance resulting from the trap state can be calculated from eqn (1) as

$$C_{it} = \left(\frac{e \cdot SS}{k_B T \ln(10)} - 1\right) C_g = (16.8 \cdot SS - 1)$$

here, C_g can be calculated as $C_g = \frac{2\pi\varepsilon_0\varepsilon}{\ln\left(\frac{4h}{d}\right)} = 3.6\ \mathrm{pF\ m^{-1}}$, where the dielectric constant for SiO_2 is ε = 3.9, and the dielectric thickness is h = 300 nm. The SWNT diameter is d = 1.4 nm. We calculated the trap state capacitance C_{it} near the conduction band (CB) and valence band (VB) to be 0.42 nF m^{-1} and 0.26 nF m^{-1}, respectively, after the deposition of 50 nm MgO. The SS for hole conduction when exposed to air is 3.3 V per decade. Thus, the VB trap capacitance before MgO deposition is calculated as 0.20 nF m^{-1}. To clearly demonstrate the effect of MgO on promoting electron conduction, these trap states are schematically plotted in Fig. 3c. The density of states for intrinsic SWNT with a diameter of 1.4 nm is also shown. The C_{it} value for CB when exposed to air is adopted from ref. 29 as 0.95 nF m^{-1} as an estimate, which is smaller than the actual value because our present device shows absolutely no electron conduction. The complete suppression of electron conduction indicates an extremely large number of trap states. This adoption is reasonable because the SWNT-dielectric surface and device structure are similar, and the VB trap state is nearly the same as in ref. 29 (0.22 nF m^{-1}). From Fig. 3c, it is clear that deposition of MgO observably decreases the trap state near the conduction band, which suppresses electron conduction.

In addition to the SS, another noteworthy feature in Fig. 3b is the large negative shift of V_{th} (ΔV_{th} = 10 V) after deposition of the MgO layer. The shift in threshold voltage is usually believed to indicate the depletion of hole carriers. The amount of charge transferred to the SWNT is 2.25×10^8 electrons per m estimated using $\Delta n = C_g \Delta V_{th}/e$.[15] Considering the diameter and atomic distance of SWNT, this value is about 0.0031 electrons per atom, where the Bravais lattice constant of 0.246 nm is used as the average carbon atom distance in SWNT. When the Fermi level is very close to the bottom of the conduction band, the electron carrier concentration can be approximated as[33]

$$n_e = \frac{4\sqrt{\pi k_B T E_g}}{\sqrt{3} a \pi \gamma_0} \quad (4)$$

where γ_0 = 2.9 eV is the nearest neighbor overlap energy, and E_g = 0.64 eV is the energy band gap for SWNT with a diameter of 1.4 nm. Because of the symmetry of SWNT energy band structure, the hole carrier concentration can also be calculated in this manner to be 2.37×10^8 m^{-1}. Therefore, the hole carriers are exactly depleted by the deposition of the MgO layer if we assume that the Fermi level is very close to the top of the valence band. We make this assumption because the transistor is a p-type when exposed to air. Starting from this point, we suppose that the deposition of the MgO layer recovers the p-type conduction to intrinsic ambipolar transport behavior. Taking the band gap into consideration, the Fermi level is increased by approximately 300 meV, which is larger than the Fermi level shift calculated by the pH value change (195 meV) of the oxygen/water couple. We assume this difference to be caused by the fact that excessive MgO also reduces the amount of the water/oxygen couple; this is not taken into account in calculation of pH value change.

Based on the above discussion, neither a single layer of MgO nor a single layer of Al_2O_3 is sufficient to convert the device from a p-type to n-type. Only the combination of MgO and Al_2O_3, forming a bilayer dielectric structure, can successfully realize carrier type conversion. We schematically illustrate the energy band diagram for the three situations in Fig. 3d. We attribute the carrier type conversion to three factors. First, the trap state near the SWNT conduction band edge is reduced because of the assimilation of water by MgO. Second, hole carriers in SWNTs are depleted because of the increase in the Fermi level of the oxygen/water redox couple as a result of an increase in its pH value. Third, the energy band of SWNT bends down because of the positive fixed charges in Al_2O_3 deposited by ALD.[22] Another important role of ALD Al_2O_3 is isolating the SWNT channel and preventing the penetration of water/oxygen species under ambient conditions, thus making the device long-term stable in air.

As stated above, the role of Al_2O_3 is providing more positive charges and passivating the SWNT channel to make it stable. Hereby, the bilayer structure of MgO/HfO_2 would also realize air-stable carrier type conversion. We have tested this speculation (Fig. S4†). Here, the HfO_2 is deposited by ALD at an even lower temperature of 90 °C. It's also interesting to see how the MgO interlayer affects the doping of CNT networks at higher temperature. This result is also presented (Fig. S5†). The successful conversions have verified our speculation and provide further evidence of the effectiveness of our proposed method.

Given the compatibility of our method with standard photolithography, it's facile to integrate both p-type and n-type transistors at the desired position on the same substrate, thus obtain complementary logic gates. As a proof of concept, we showed a CMOS inverter in Fig. 4a. The n-type transistor is obtained by MgO/Al_2O_3 coating, patterned by photolithography and lift-off process. The back-gate is used as input terminal, and the common drain pad is used as output terminal. At a supply voltage of 3.5 V, the inverter shows maximum voltage gain of 11.

For FETs based on individual SWNT or SWNT parallel arrays, it is well known that the Schottky barrier present at the metal–SWNT contact controls the carrier injection into the SWNT channel.[34] Selection of different metals as the source–drain electrode has been reported to switch the polarity of individual SWNT FETs.[16] The metal Pd has commonly been chosen as an electrode to fabricate p-type FETs on parallel SWNTs.[35]

Here, we fabricated devices with Pd and Au electrodes in our proposed n-type frame. The results are shown in Fig. 5.

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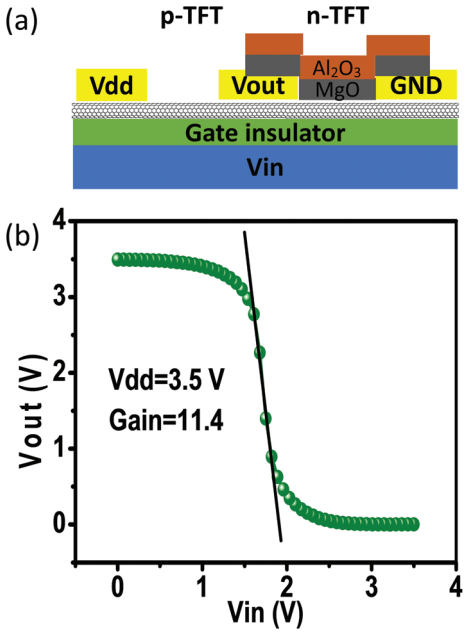

Fig. 4 (a) Schematics of a complementary inverter. (b) Transfer characteristics of the inverter. Both the channel length and channel width are 40 μm for both the n-type and p-type device. The gate insulator is 40 nm HfO_2. The thickness of MgO and Al_2O_3 are 10 nm and 30 nm respectively.

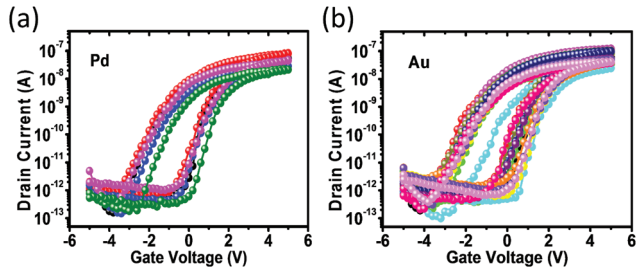

Fig. 5 Transfer characteristics of n-type CNT-TFTs with Pd (a) and Au (b) as drain/source metal contact materials measured at V_{DS} = 2 V in air. The channel dimensions are 40 μm × 40 μm for all the devices.

The devices with Pd metal pads show n-type behavior, with no observable difference from the devices with an Au source–drain pad. When the channel is exposed to air, all the devices exhibited p-type characteristics, whether with Au or Pd pads. This indicates that the Schottky barrier at the metal–SWNT contact does not play a dominant role in CNT-TFTs, because the conduction path in the percolation network consists of many SWNT–SWNT junctions. These numerous junctions contribute a large resistance to the device. Therefore, we suggest that the doping of the SWNT in the TFT channel plays a more important role than the Schottky barrier at the metal–SWNT contact in determining the transport behavior of TFTs.

It's known that oxygen molecules in air can induce an equivalent dipole near the source and drain contacts, thereby

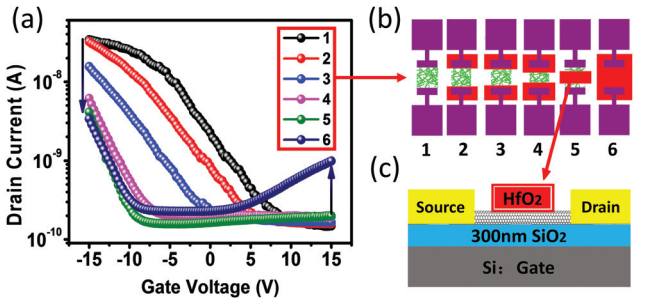

Fig. 6 Effect of doping of the CNT-TFT channel on the electrical transport characteristics. (a) Transfer characteristics of CNT-TFTs with ALD HfO_2 partially covering the transistor. (b) The device configuration corresponding to each curve in (a). The red area represents HfO_2, which are 2 μm × 2, 4 μm × 2, 10 μm × 2 and 20 μm for devices #2, #3, #4, and #5 respectively. (c) Schematic diagram of the device structure.

pinning the Fermi level close to the valence band at the metal–SWNT contact in individual-SWNT-based transistors.[22,26,36] To further investigate the role of the metal–SWNT contact and the doping of SWNT in the channel on influencing the electrical properties of CNT-TFTs, we fabricated a series of devices, as shown in Fig. 6. The general device structure is schematically displayed in Fig. 6c. The specific device layout corresponding to each measurement curve is shown in Fig. 6b. The purple area in Fig. 6b represents the metal electrode, and the red area represents the HfO_2 layer deposited by ALD at 90 °C. The role of the HfO_2 layer is to partially remove the adsorbates on the carbon nanotubes. The channel length is 40 μm. The width of the HfO_2 area in the channel length direction is 2 μm × 2, 4 μm × 2, 10 μm × 2 and 20 μm for devices #2, #3, #4, and #5 respectively. It can be seen that ALD HfO_2 has an effect of reducing the hole current while promoting the electron current, yet cannot convert the device to n-type. The hole conduction decreases proportionally with increasing HfO_2 covered area from device #2 to device #4. When HfO_2 covers merely the contact area in device #2, the hole current decreases slightly compared to the entirely exposed one in device #1. Furthermore, when HfO_2 covers the same area but with a different position in the channel, the devices show similar transport behaviour (device #4 and device #5). Therefore, we believe that the doping of SWNTs in the channel plays a dominant role in determining the electrical characteristics of CNT-TFTs, unlike the FET based on individual SWNT, in which the barrier at the metal–SWNT contact determines the device electrical characteristics.

Conclusions

We have fabricated top-gated n-type carbon nanotube thin-film transistors on flexible substrates through a photolithography compatible low temperature method. The particular feature of this method is the use of a gate dielectric of bilayered structure, *i.e.* an e-beam evaporated MgO layer accompanied by an

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ALD Al_2O_3 or HfO_2 layer. The advantage of this method is the low temperature required, *i.e.* 120 °C or 90 °C and the compatibility with the lift-off process. The mechanism of carrier type conversion is attributed to the hole depletion in SWNT, the decrease of the trap state density by MgO assimilating adsorbed water molecules in the vicinity of SWNT, and the energy band bending due to the positive fixed charge in the ALD layer, as determined by a series of control experiments. The calculated amount of depleted holes based on the measurement is consistent with the number of holes indicated by a theoretical estimate based on the SWNT density of state and Fermi distribution. The as-fabricated device is long-term stable in air, which originates from the ALD layer. We also demonstrated that doping of the SWNT network in the channel plays a more important role than the Schottky contact in determining the transport properties of CNT-TFTs, unlike the situation in individual-SWNT-based transistors.

Experimental

SWNTs (NanoIntegris Inc.) were dispersed in *N*-methyl-2-pyrrolidone (Sigma-Aldrich). The semiconductor purity was 99% and the mean diameter was 1.4 nm. The substrate surface was functionalized with 3-aminopropyltriethoxysilane (APTES, Sigma-Aldrich). The heavily doped silicon substrate has a thermal SiO_2 layer of 300 nm. The PET substrate was coated with 50 nm of SiO_2 by e-beam deposition before functionalization. Random networks of SWNTs were deposited by immersing the functionalized substrate into the SWNT solution for 30 min. Subsequently, the drain and source electrodes were defined by standard photolithography and e-beam evaporation followed by a lift-off process. After drain and source forming, the active channel regions were defined and isolated by photolithography and O_2 plasma etching. Then, the gate dielectric layer or passivation layer were patterned by photolithography and formed by film deposition, followed by lift-off. MgO was deposited by e-beam evaporation, and Al_2O_3 and HfO_2 were deposited using ALD at 120 °C and 90 °C, respectively, finally forming the gate electrode. All electrical measurements were performed with an Agilent semiconductor analyzer 4156C at a Lakeshore probe station under ambient atmosphere at room temperature.

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Notes and references

1 T. Dürkop, S. A. Getty, E. Cobas and M. S. Fuhrer, *Nano Lett.*, 2004, **4**, 35–39.
2 Z. Yao, C. L. Kane and C. Dekker, *Phys. Rev. Lett.*, 2000, **84**, 2941–2944.
3 Q. Cao, H. Kim, N. Pimparkar, J. P. Kulkarni, C. Wang, M. Shim, K. Roy, M. A. Alam and J. A. Rogers, *Nature*, 2008, **454**, 495–500.
4 L. Ding, Z. Zhang, S. Liang, T. Pei, S. Wang, Y. Li, W. Zhou, J. Liu and L. Peng, *Nat. Commun.*, 2012, **3**, 677.
5 C. Wang, J. Chien, K. Takei, T. Takahashi, J. Nah, A. M. Niknejad and A. Javey, *Nano Lett.*, 2012, **12**, 1527–1533.
6 C. Wang, J. Zhang and C. Zhou, *ACS Nano*, 2010, **4**, 7123–7132.
7 M. M. Shulaker, G. Hills, N. Patil, H. Wei, H. Chen, H. S. P. Wong and S. Mitra, *Nature*, 2013, **501**, 526–530.
8 A. D. Franklin, M. Luisier, S. Han, G. Tulevski, C. M. Breslin, L. Gignac, M. S. Lundstrom and W. Haensch, *Nano Lett.*, 2012, **12**, 758–762.
9 D. Bozovic, M. Bockrath, J. H. Hafner, C. M. Lieber, H. Park and M. Tinkham, *Phys. Rev. B: Condens. Matter*, 2003, **67**, 033407.
10 R. H. Reuss, B. R. Chalamala, A. Moussessian, M. G. Kane, A. Kumar, D. C. Zhang, J. A. Rogers, M. Hatalis, D. Temple, G. Moddel, B. J. Eliasson, M. J. Estes, J. Kunze, E. S. Handy, E. S. Harmon, D. B. Salzman, J. M. Woodall, M. A. Alam, J. Y. Murthy, S. C. Jacobsen, M. Olivier, D. Markus, P. M. Campbell and E. Snow, *Proc. IEEE*, 2005, **93**, 1239–1256.
11 M. Radosavljevic, J. Appenzeller, P. Avouris and J. Knoch, *Appl. Phys. Lett.*, 2004, **84**, 3693–3695.
12 A. Javey, R. Tu, D. B. Farmer, J. Guo, R. G. Gordon and H. Dai, *Nano Lett.*, 2005, **5**, 345–348.
13 M. Shim, A. Javey, N. W. Shi Kam and H. Dai, *J. Am. Chem. Soc.*, 2001, **123**, 11512–11513.
14 S. M. Kim, J. H. Jang, K. K. Kim, H. K. Park, J. J. Bae, W. J. Yu, I. H. Lee, G. Kim, D. D. Loc, U. J. Kim, E. Lee, H. Shin, J. Choi and Y. H. Lee, *J. Am. Chem. Soc.*, 2009, **131**, 327–331.
15 H. Kim, E. Jeon, J. Kim, H. So, H. Chang, J. Lee and N. Park, *Appl. Phys. Lett.*, 2008, **93**, 123106.
16 Z. Zhang, X. Liang, S. Wang, K. Yao, Y. Hu, Y. Zhu, Q. Chen, W. Zhou, Y. Li, Y. Yao, J. Zhang and L. Peng, *Nano Lett.*, 2007, **7**, 3603–3607.
17 L. Ding, S. Wang, Z. Zhang, Q. Zeng, Z. Wang, T. Pei, L. Yang, X. Liang, J. Shen, Q. Chen, R. Cui, Y. Li and L. Peng, *Nano Lett.*, 2009, **9**, 4209–4214.
18 D. Shahrjerdi, A. D. Franklin, S. Oida, J. A. Ott, G. S. Tulevski and W. Haensch, *ACS Nano*, 2013, **7**, 8303–8308.
19 A. Kojima, M. Shimizu, C. K. Hyon, T. Kamimura, M. Maeda and K. Matsumoto, *Jpn. J. Appl. Phys.*, 2005, **44**, L328–L330.
20 T. Ha, K. Chen, S. Chuang, K. M. Yu, D. Kiriya and A. Javey, *Nano Lett.*, 2015, **15**, 392–397.
21 N. Moriyama, Y. Ohno, T. Kitamura, S. Kishimoto and T. Mizutani, *Nanotechnology*, 2010, **21**, 165201.
22 J. Zhang, C. Wang, Y. Fu, Y. Che and C. Zhou, *ACS Nano*, 2011, **5**, 3284–3292.

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23 L. Suriyasena Liyanage, X. Xu, G. Pitner, Z. Bao and H. S. P. Wong, *Nano Lett.*, 2014, **14**, 1884–1890.
24 P. Gao, J. Zou, H. Li, K. Zhang and Q. Zhang, *Small*, 2013, **9**, 813–819.
25 S. Kumar, N. Pimparkar, J. Y. Murthy and M. A. Alam, *Appl. Phys. Lett.*, 2006, **88**, 123505.
26 V. Derycke, R. Martel, J. Appenzeller and P. Avouris, *Appl. Phys. Lett.*, 2002, **80**, 2773.
27 H. Imaeda, S. Ishii, S. Kishimoto, Y. Ohno and T. Mizutani, *Jpn. J. Appl. Phys.*, 2012, **51**, 02BN06.
28 C. M. Aguirre, P. L. Levesque, M. Paillet, F. Lapointe, B. C. St-Antoine, P. Desjardins and R. Martel, *Adv. Mater.*, 2009, **21**, 3087–3091.
29 Q. Qian, G. Li, Y. Jin, J. Liu, Y. Zou, K. Jiang, S. Fan and Q. Li, *ACS Nano*, 2014, **8**, 9597–9605.
30 S. Myung, S. Woo, J. Im, H. Lee, Y. S. Min, Y. K. Kwon and S. Hong, *Nanotechnology*, 2010, **21**, 345301.
31 S. Myung, J. Park, H. Lee, K. S. Kim and S. Hong, *Adv. Mater.*, 2010, **22**, 2045.
32 L. Yan, C. M. Lopez, R. P. Shrestha, E. A. Irene, A. A. Suvorova and M. Saunders, *Appl. Phys. Lett.*, 2006, **88**, 142901.
33 J. Liang, D. Akinwande and H. S. P. Wong, *J. Appl. Phys.*, 2008, **104**, 64515.
34 S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller and P. Avouris, *Phys. Rev. Lett.*, 2002, **89**, 106801.
35 A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom and H. Dai, *Nano Lett.*, 2004, **4**, 1319–1322.
36 R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K. K. Chan, J. Tersoff and P. Avouris, *Phys. Rev. Lett.*, 2001, **87**, 256801–256805.